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Issued by(Last revised)	Reviewed by	Approved by	Document Administrator

WM-N500JS

Hardware Manual

Version 1.5

Contents

■ Revision History

All revisions made to this document are listed below;

Version	Date	Description	Issued by
1.4	2021-12-20	*Initial release for Soft Bank in Japan*	Alex choi
1.5	2022-03-20	Update User guide	MY Cho

1. Product Overview

1.1. WM-N500JS series:

- ✓ Qualcomm MDM9206 chipset base

<Model name and Features>

Model Name	Carrier	LTE BAND	CATEGORY	MEMORY (MCP)	S/W
WM-N502JS		B1, B8	M1 only	4Gb NAND Flash / 2Gb DDR2	Linux

Frequency bands:

- ✓ LTE B1 – TX : 1920 ~1980MHz, LTE – RX : 2110~2170MHz MHz
- ✓ LTE B8 – TX : 880~915MHz, LTE – RX : 925~960MHz

1.2. Contents and Function

1) Model Name: WM-N500JS
2) Target User: IoT Users
3) Network:
   - ✓ Data only
   - ✓ LTE Cat.M1: Band8, Band1
   - ✓ GPS(Optional): 1574.4MHz ~ 1605.9MHz
4) RF Power: Power Class III

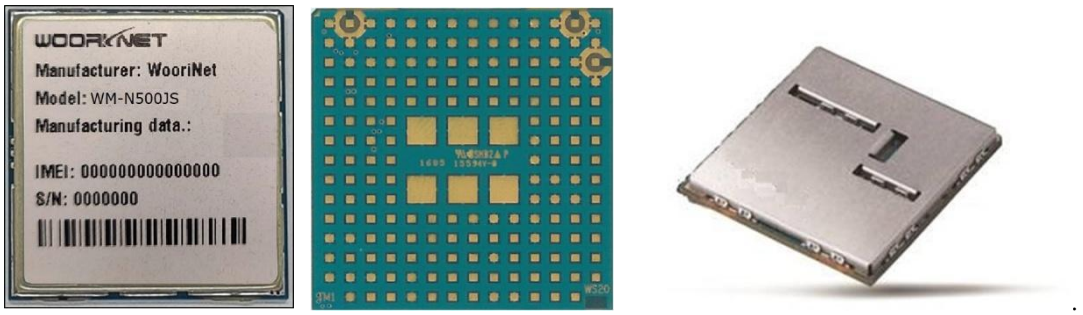
2. Product Specification and Characteristics

2.1. HW / Dimension

<HW Features>

Items	Specifications	Remark
Chipset	Qualcomm MDM9206	
Memory (MCP)	NAND Flash+ DDR2	
USIM Interface	External USIM (PIN OUT)	
Connectivity	UART 2EA / SPI 1EA / I2C 1 EA GPIO USB 2.0 / UIM / JTAG	
Air Interface	LTE : Band1 , Band8	
Antenna	PIN OUT Type	
Power consumption (Max. current)	550 mA (@ Tx Max Power 23dBm ±0.4dB, +4.0V)	@ LTE B8
Operating Voltage	+3.4 Vdc ~ +4.2 Vdc	
Dimension / Weight	26.6 x 28.0 X 2.7 (mm) (약 6.8g)	
Operating Temperature & Humidity	-20℃ ~ +60℃ / 95% (@+60℃)	

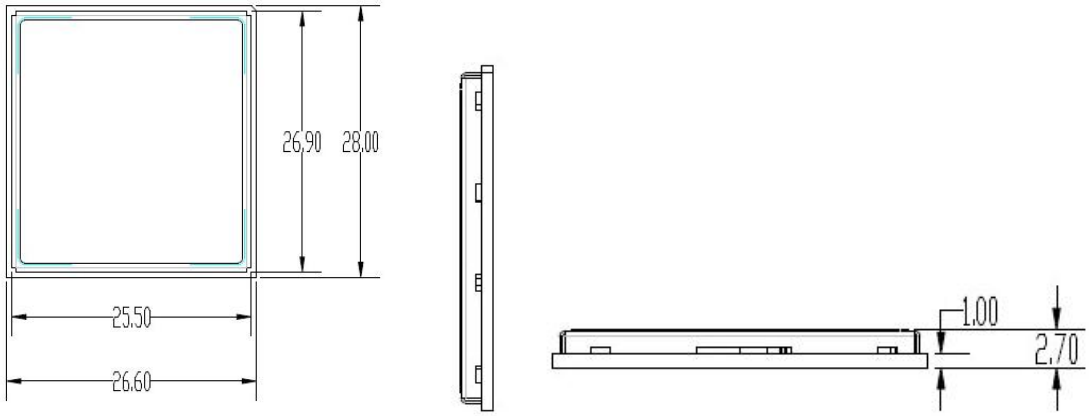
2.2. Exterior photos



<TOP> <BOTTOM>

<Picture 2.2 WM-N500JS>

2.3. Exterior Drawing



<Picture 2.3 WM-N500JS Exterior Drawing>

2.4. Module characteristic

2.4.1. Electrical properties

<Electrical properties>

Parameter	Description	Min.	Typ.	Max.	Units
V_Batt	Power Supply Voltage	3.4	4.0	4.2	V
Iv_batt	Power Supply Current	550	-		mA
Traffic current	Power save mode (PSM)	-	7.3	-	uA
	IDLE	-	0.79	-	mA
	Tx Max Power 23dBm ±0.4dB, +4.0V)	450	500	550	mA
Power off	Average of power off current consumption	5.3		10	uA
VIH	High-level Input Voltage, CMOS	1.17	1.8	2.1	V
VIL	Low-level Input Voltage, CMOS	-0.3	-	0.63	V
VOH	High-level Output Voltage, CMOS	1.35	-	1.8	V
VOL	Low-level Output Voltage, CMOS	0	-	0.45	V

2.4.2. Reliability characteristic

<Reliability characteristic>

ITEM	Specification
Storage Temperature	-40℃ to + 85℃
Operating Temperature	-20℃ to + 60℃
Humidity (Operating)	95%(60℃) relative humidity (non-condensing)
Vibration (Operating)	10 Hz to 100 Hz sinusoidal, 1.0G
Drop	No damages after 75cm drop over concrete floor

2.4.3. RF characteristic

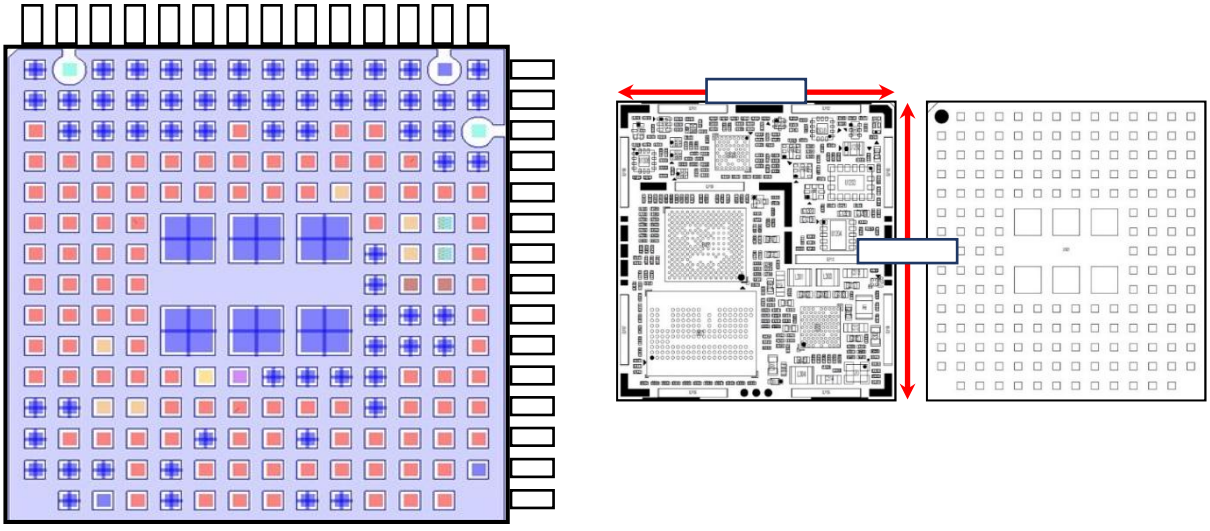
< RF characteristic>

ITEM	Condition				
	BW	DL conf	UL conf		Specification
			Mod	RB	
Maximum Output Power (Class 3)	1.4MHz 3MHz 5MHz 10MHz 15MHz 20MHz	NA	QPSK	5MHz 1 RB 10MHz 1,4 RB 15MHz 1,6 RB 20MHz 1,6 RB	+23 dBm ±2.7dB
Minimum Output Power	1.4MHz 3MHz 5MHz 10MHz 15MHz 20MHz	NA	QPSK	5MHz 6 RB	< -40 dBm

Frequency Error	5MHz	QPSK 4RB	QPSK	6 RB	±0.1ppm @ Band 5,8 ±0.2ppm @ Band 1,3
EVM	5MHz	NA	QPSK	1,6 RB	< 17.5%
			16QAM	1,5 RB	< 12.5%
Maximum Input Level	5MHz	16QAM 2RB	QPSK	6	> -25.7dBm
Reference Sens. Level	5MHz	QPSK 4RB	QPSK	6	< -102.3dBm @ Band1 < -99.3dBm @ Band3 < -100.8dBm @ Band5 < -99.8dBm @ Band8

✓ RF Spec 3GPP TS36.521 Support.

2.5. Pin Assignment



< BOTTOM VIEW >

<Picture 2.5 WM-N500JS Pin Assignment>

2.6. I/O parameter definitions

<Chart 2.6 WM-N500JS I/O parameter definitions>

Symbol	Description
Pad attribute	
PI	Power input
PO	Power output
B	Bidirectional digital
DI	Digital input
DO	Digital output

AI	Analog input
AO	Analog output
AIO	Analog input, output
Pad voltage	
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (2.85 V),
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.85 V)
P6	Pad group 6 (UIM2 and MDIO); tied to VDD_P6 pins (1.8 V or 2.85 V)
P8	Pad group 8 (HSIC); tied to VDD_P8 pins (1.2 V)

2.7. Pin Description

<WM-N500JS Pin Description >

Signal Name	PAD No.	I/O	Voltage	Functional description
Power				
VBAT	F14,F15,G14,G15, H14,H15	Pi	4.0V	Main Power Supply
GND	A1,A2,A12,A13,A14, B2,B3,B12,B14,B15, C1,C2,C3,C14,D1, D2,D3,E1,E2,E3,E6,	-	-	

	E9,E14,E15,F1,F2, F3,G1,G2,G6,G9,H1, H2,H3,H11,J1,J2,J3, J6,J9,J11,J13,J15,K1, K2,K11,K15,L1,L2,L7 ,L8,L9,L10,L11,L12, M1,M2,M3,M9,M10 , N2,N3,N4,N9,N10, P1,P2,P4,			Ground
VREG_L13_2P85	D15	PO	P2	2.85V Regulated Voltage for reference voltage or customer's use case
VREG_L11_1P8	H12	PO	P3	1.8V Regulated Voltage for reference voltage or customer's use case
Power Control				
CBL_PWR_N	B8	DI	-	Power On Signal (Active Low)
PMD_RESIN_N	E13	DI	-	Reset/
UART Interface				
UART2_TX	E5	DO	P3	UART TX
UART2_RX	F5	DI	P3	UART RX
UART2_CTS	E4	DI	P3	UART CTS
UART2_RFR	F4	DO	P3	UART RFR
UART5_TX	A3	DO	P3	UART TX
UART5_RX	A4	DI	P3	UART RX
SPI Interface				
SPI_MOSI	D8	DO	P3	SPI_MOSI
SPI_MISO	D9	DI	P3	SPI_MISO
SPI_CS_N	C8	DO	P3	SPI_CS_N
SPI_CLK	D7	DO	P3	SPI_CLK

External USIM Interface				
VREG_L6_UIM1	C13	PO	P5	External USIM Power
UIM1_RESET	M5	DO	P5	External USIM Reset
UIM1_PRESENT	M4	DI	P3	External USIM Detect
UIM1_CLK	L5	DO	P5	External USIM Clock
UIM1_DATA	L4	B	P5	External USIM Data
USB Interface				
USB_VBUS	H13	PI	5V	USB Power Supply
USB_ID	P8	AI	-	USB High speed ID
USB_HS_DM	N8	AIO	-	USB High-speed differential data
USB_HS_DP	M8	AIO	-	USB High-speed differential data
SDIO Interface				
SDC2_DATA3	B10	B	P2	Secure digital controller2 databit3
SDC2_DATA2	C9	B	P2	Secure digital controller2 databit2
SDC2_DATA1	A9	B	P2	Secure digital controller2 databit1
SDC2_DATA0	B9	B	P2	Secure digital controller2 databit0
SDC2_CLK	C10	B	P2	Secure digital controller2 clock
SDC2_CMD	A10	B	P2	Secure digital controller2
I2C Interface				
I2C_SDA	L3	B	P3	I2C data
I2C_SCL	K3	B	P3	I2C Clock
JTAG Interface				
MDM_JTAG_PS_HOL	B4	DI	P3	JTAG PSHOLD
MDM_JTAG_SRST_N	B6	DI	P3	JTAG reset for debug
MDM_JTAG_TCK	B7	DI	P3	JTAG clock input
MDM_JTAG_TMS	B5	B	P3	JTAG mode select input
MDM_JTAG_TDI	A6	DI	P3	JTAG data input

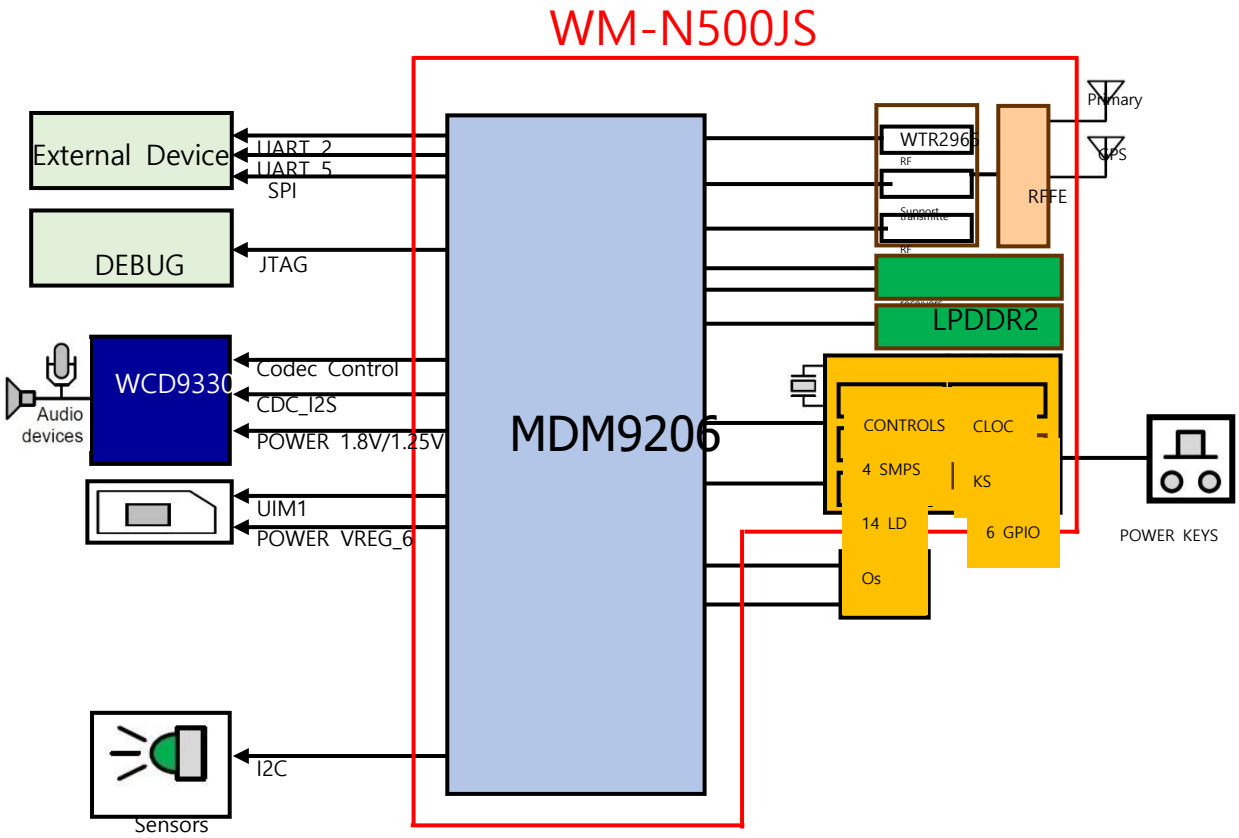
MDM_JTAG_TDO	A7	DO	P3	JTAG data output
MDM_JTAG_TRST_N	A5	DI	P3	JTAG reset
RF IN/OUT				
ANT_MAIN	B1	RF	-	MAIN(Primary) Antenna IN/OUT
ANT_GPS	N1	RF	-	GPS Antenna IN
GPIO				
LED2	B13	DO	1.8V	GPIO for Power monitor LED
SDC1_DATA1	M12	DO	P3	GPIO for LED control
SDC1_DATA2	N12	DO	P3	GPIO for LED control
RS232_SHDN_N	D14	DO	1.8V	GPIO for RS232 shutdown
EMG_DL_N	A8	DI	P3	Emergency Download key input wakeup interrupt GPIO
GPIO_76	H5	DO	P3	General GPIO
GPIO_77	J5	DO	P3	General GPIO
GPIO_78	K5	DO	P3	General GPIO
GPIO_79	G5	DO	P3	General GPIO
NC				
PMD_MPP01_ADC	D13	-	-	RESERVED (These pins are reserved for specific application. It needs to be discussed for use cases.)
PON_TRIG	E12	-	-	
BATT_ID	G12	-	-	
HW_ADC	F13	-	-	
SPMI_CLK	C12	-	-	
SPMI_DATA	D12	-	-	
HSIC_STB	P9	-	-	
HSIC_DATA	P10	-	-	
ANT_MIMO	P3	-	-	
BT_EN	C11	-	-	

LCD_1P8_EN	B11	-	-	RESERVED (These pins are reserved for specific application. It needs to be discussed for use cases.)
WLAN_SLEEP_CLK	F11	-	-	
RFCLK2_QCA	D11	-	-	
VREG_L2_1P8	G13	-	-	
VREG_L5_UIM2	P7	-	-	
VREG_L9_1P225	G11	-	-	
VREG_S4_1P95	C15	-	-	
LTE_COEX_TX_UART	C7	-	-	
LTE_COEX_RX_UART	C6	-	-	
SDC1_CLK	P12	-	-	
SDC1_CMD	N11	-	-	
SDC1_DATA0	P11	-	-	
SDC1_DATA3	M11	-	-	
I2S_MCLK_AD2	G3	-	-	
MI2S_1A_SCLK	K4	-	-	
MI2S_1A_WS	G4	-	-	
MI2S_1A_D0	H4	-	-	
MI2S_1A_D1	J4	-	-	
RST_WCD_9330	D4	-	-	
CODEC_INT	C4	-	-	
SLIC_RST_N	D6	-	-	
SLIC_INT_N	D5	-	-	
PROXIMITY_INT_N	K12	-	-	
WAKE_ON_WIRELES	E11	-	-	
EBI2_CLE_N	N13	-	-	
EBI2_OE_N	P14	-	-	
EBI2_WE_N	L13	-	-	

EBI2_A_D0	M14	-	-	RESERVED (These pins are reserved for specific application. It needs to be discussed for use cases.)
EBI2_A_D1	P13	-	-	
EBI2_A_D2	L14	-	-	
EBI2_A_D3	M13	-	-	
EBI2_A_D4	M15	-	-	
EBI2_A_D5	N14	-	-	
EBI2_A_D6	L15	-	-	
EBI2_A_D7	N15	-	-	
SGMII_TX_P	N7	-	-	
SGMII_TX_M	M7	-	-	
SGMII_RX_P	N6	-	-	
SGMII_RX_M	M6	-	-	
SGMII_CLK	L6	-	-	
SGMII_DATA	N5	-	-	
EPHY_RST_N	P5	-	-	
EPHY_INT_N	P6	-	-	
WLAN_EN	D10	-	-	
GRFC_2	J12	-	-	
GRFC_5	K13	-	-	
GRFC_10	C5	-	-	
NC	A11,F12,J14,K14	-	-	No internal connection

3. Block Diagram

3.1. Application & System Block diagram



<Picture 3.1 WM-N500JS Block diagram >

4. System Interface

4.1. Modem Power supply

<WM-N500JS Power interface >

PAD	Signal Name	I/O	Voltage	Functional description
F14	VBAT	PI	4.0V	External Power Supply
F15	VBAT	PI	4.0V	External Power Supply
G14	VBAT	PI	4.0V	External Power Supply
G15	VBAT	PI	4.0V	External Power Supply
H14	VBAT	PI	4.0V	External Power Supply
H15	VBAT	PI	4.0V	External Power Supply
D15	VREG_L13_2P85	PO	P2	2.85V Regulated Voltage for reference voltage or customer's use case
H12	VREG_L11_1P8	PO	P3	1.8V Regulated Voltage for reference voltage or customer's use case

4.2. Modem Power Control (Power on/off)

<WM-N500JS Power control interface >

PAD	Signal Name	I/O	Voltage	Functional description
B8	CBL_PWR_N	DI	-	Power On Signal (Active Low)
E13	PMD_RESIN_N	DI	-	HW Reset (Active Low)

4.3. UART Interface

UART2 : AT command

<WM-N500JS UART interface >

PAD	Signal Name	I/O	Voltage	Functional description
UART2 : Modem AT command UART				
E5	UART2_TX	DO	P3	High-speed UART transmit data output
F5	UART2_RX	DI	P3	High-speed UART receive data input
E4	UART2_CTS	DI	P3	High-speed UART clear to send signal
F4	UART2_RFR	DO	P3	UART1 ready for receive signal
UART5 : Console UART				
A3	UART5_TX	DO	P3	UART TX
A4	UART5_RX	DI	P3	UART RX

4.4. SPI Interface

<WM-N500JS SPI interface >

PAD	Signal Name	I/O	Voltage	Functional description
D8	SPI_MOSI	DO	P3	SPI_MOSI
D9	SPI_MISO	DI	P3	SPI_MISO
C8	SPI_CS_N	DO	P3	SPI_CS_N
D7	SPI_CLK	DO	P3	SPI_CLK

4.5. External USIM Interface

<WM-N500JS USIM interface >

PAD No.	Signal Name	I/O	Voltage	Functional description
C13	VREG_L6_UIM1	PO	P5	USIM Power
M5	UIM1_RESET	DO	P5	USIM Reset
M4	UIM1_PRESENT	DI	P3	UIM Detection
L5	UIM1_CLK	DO	P5	UIM Clock
L4	UIM1_DATA	B	P5	UIM Data

4.6. USB Interface

USB2.0 HS Support.

<WM-N500JS USIM interface >

PAD No.	Signal Name	I/O	Voltage	Functional description
H13	USB_VBUS	PI	5V	USB Power Supply
P8	USB_ID	AI	-	USB ID
N8	USB_HS_DM	AIO	-	High-speed USB differential data, (-)
M8	USB_HS_DP	AIO	-	High-speed USB differential data, (+)

4.7. SDIO Interface

<WM-N500JS SDIO interface >

PAD	Signal Name	I/O	Voltage	Functional description
B10	SDC2_DATA3	B	P2	Secure digital controller2 databit3

C9	SDC2_DATA2	B	P2	Secure digital controller2 databit2
A9	SDC2_DATA1	B	P2	Secure digital controller2 databit1
B9	SDC2_DATA0	B	P2	Secure digital controller2 databit0
C10	SDC2_CLK	B	P2	Secure digital controller2 clock
A10	SDC2_CMD	B	P2	Secure digital controller1 command

4.8. I2C Interface

<WM-N500JS I2C interface >

PAD	Signal Name	I/O	Voltage	Functional description
L3	I2C_SDA	B	P3	I2C data
K3	I2C_SCL	B	P3	I2C Clock

4.9. JTAG Interface

<WM-N500JS JTAG interface >

PAD	Signal Name	I/O	Voltage	Functional description
B4	MDM_JTAG_PS_HOLD	DI	P3	JTAG PSHOLD
B6	MDM_JTAG_SRST_N	DI	P3	JTAG reset for debug
B7	MDM_JTAG_TCK	DI	P3	JTAG clock input
B5	MDM_JTAG_TMS	B	P3	JTAG mode select input
A6	MDM_JTAG_TDI	DI	P3	JTAG data input
A7	MDM_JTAG_TDO	DO	P3	JTAG data output
A5	MDM_JTAG_TRST_N	DI	P3	JTAG reset

4.10. Antenna Interface

<Chart 4.10 WM-N500JS Antenna interface >

PAD	Signal Name	I/O	Voltage	Functional description
B1	ANT_MAIN	RF	-	MAIN(Primary) Antenna IN/OUT
N1	ANT_GPS	RF	-	GPS Antenna IN

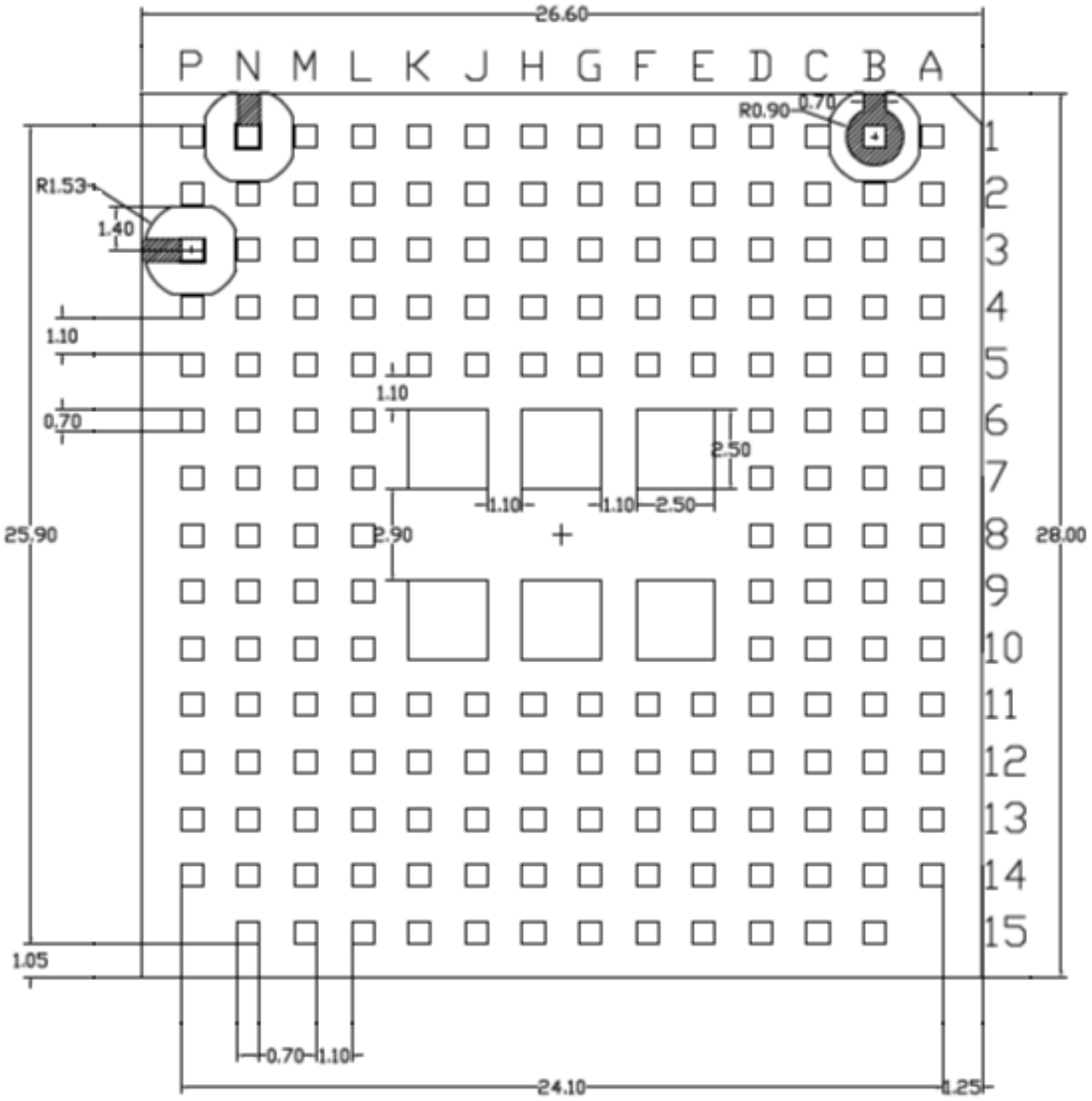
4.11. GPIO Interface

<WM-N500JS GPIO interface >

PAD	Signal Name	I/O	Voltage	Functional description
B13	LED2	DO	1.8V	GPIO for Power monitor LED control
M12	SDC1_DATA1	DO	P3	GPIO for LED control
N12	SDC1_DATA2	DO	P3	GPIO for LED control
D14	RS232_SHDN_N	DO	1.8V	GPIO for RS232 shutdown
A8	EMG_DL_N	DI	P3	Emergency Download key input Wakeup interrupt GIPI
H5	GPIO_76	DO	P3	General GPIO
J5	GPIO_77	DO	P3	General GPIO
K5	GPIO_78	DO	P3	General GPIO
G5	GPIO_79	DO	P3	General GPIO

5. PCB LANDPATTERN

5.1. Recommended PCB Land Pattern

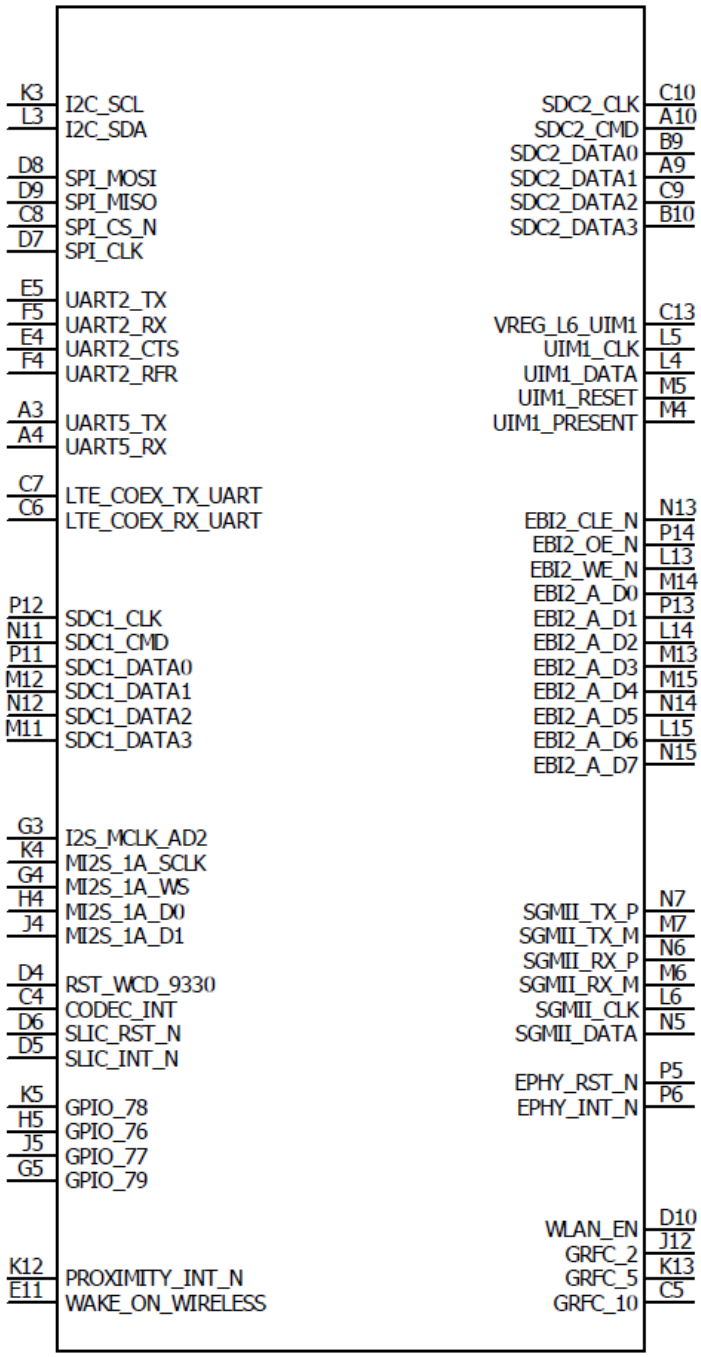


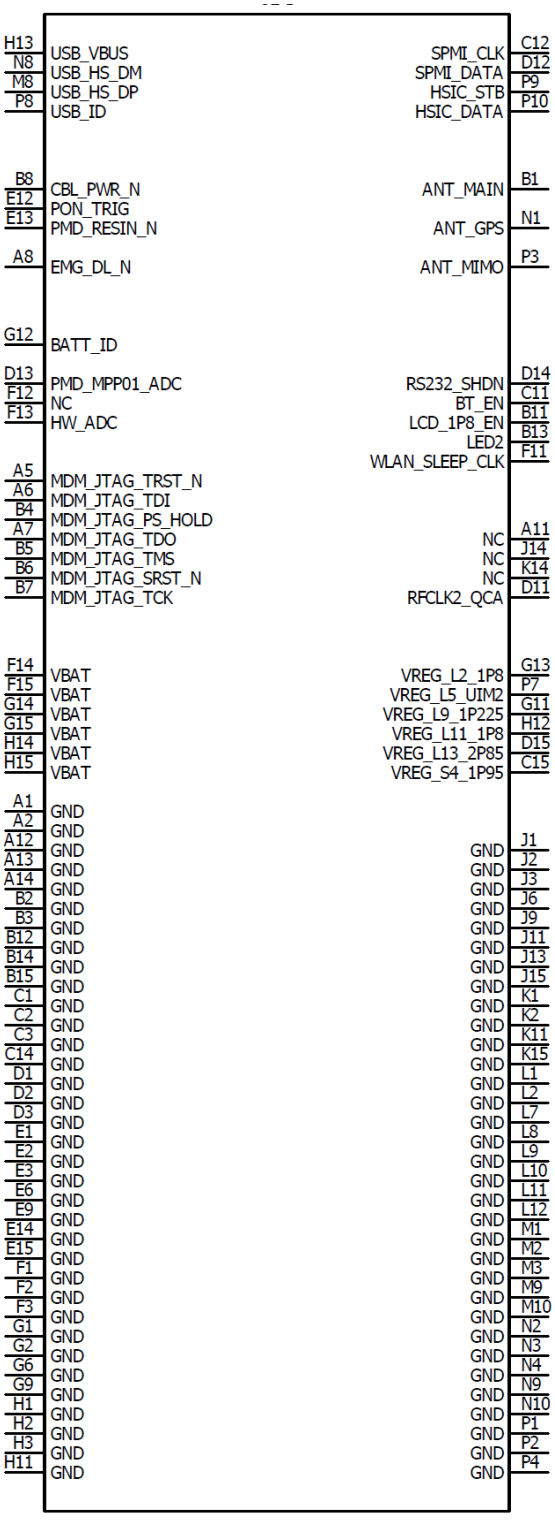
< TOP VIEW >

<Picture 5.1 WM-N500JS PCB LAND PATTERN >

6. User Guide

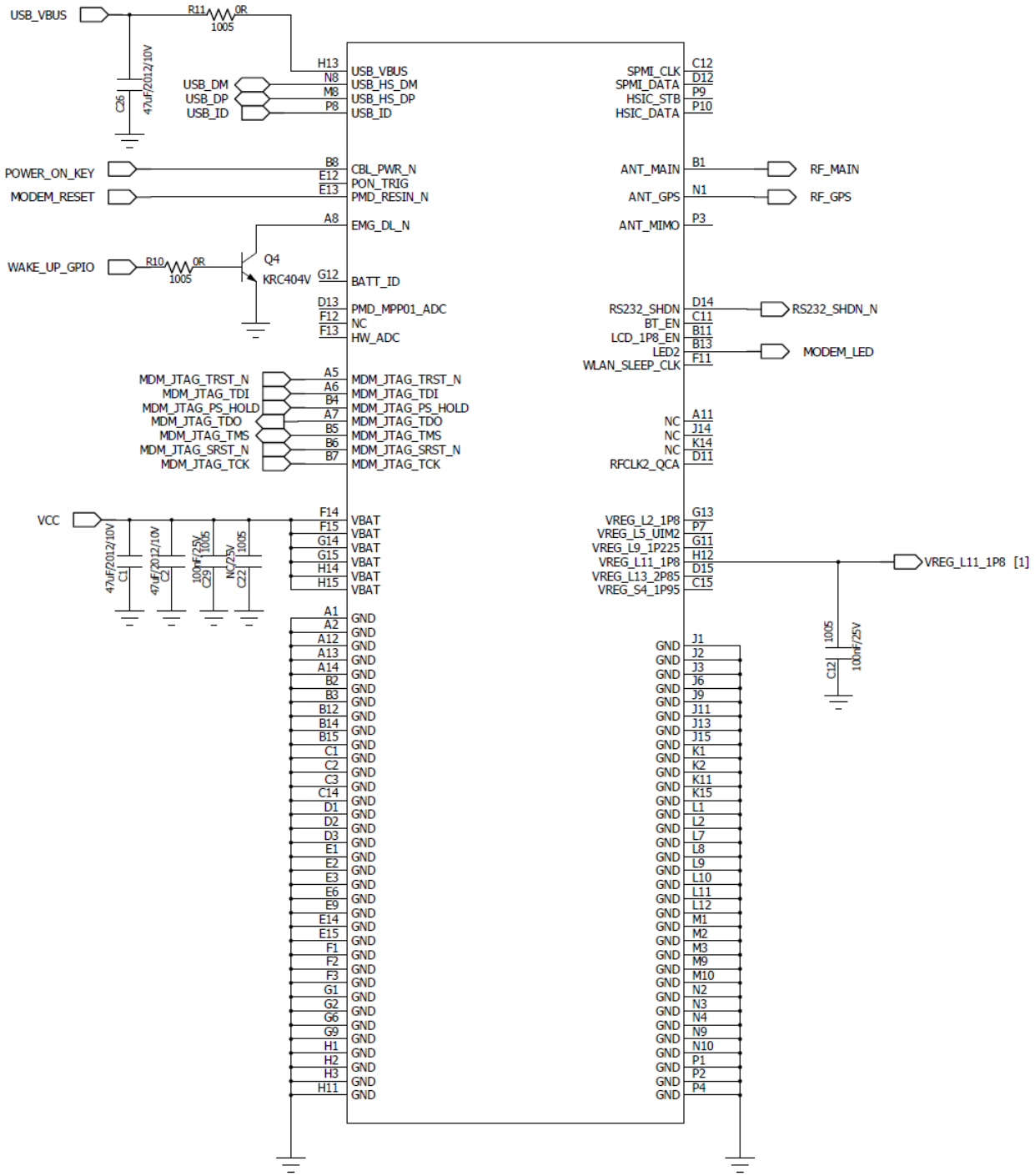
6.1. WM-N500JS LGA Pin Out

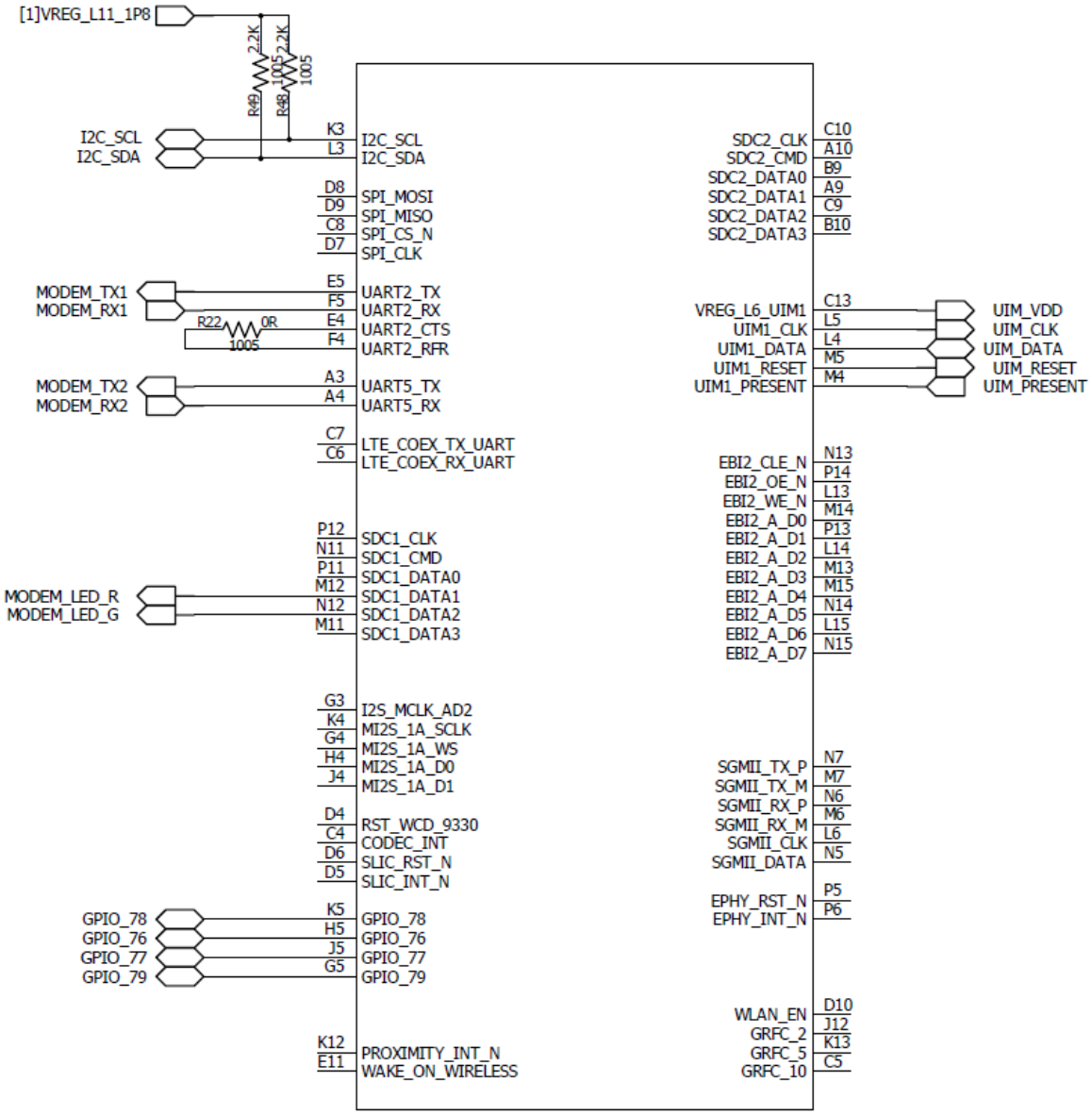




<Picture 6.1 WM-N500JS LGA PIN OUT >

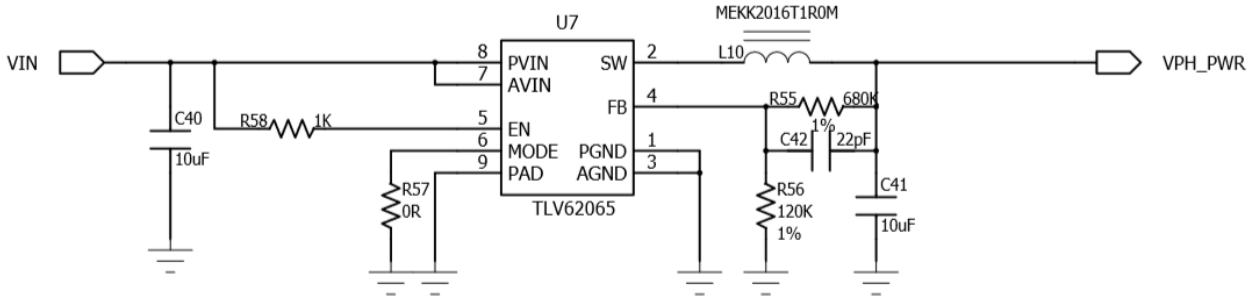
6.2. Reference Schematic





<Picture 6.2 WM-N500JS Reference schematic >

6.3. Power supply

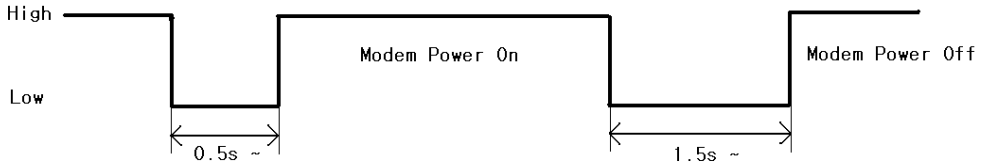


< Picture 6.3 Power Source example >

The module utilizes a single regulated power rail of DC typical 4.0V. The 4.0V power rail source must support to 550mA or more current. The module power must be supported to an independent power source. Noise, leakage current of output voltage and protection circuit should be considered when designing the power source.

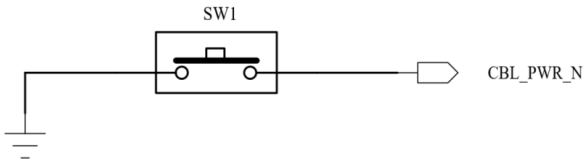
6.4. Power On Key

Picture 6.4.1 is power on sequence. CBL_PWR_N(pin B8) signal is an Active Low input that is used to turn on/off the module. When the input signal is Low for more than 0.5 sec while the module is turned off, the Module will be turned on. Conversely, When the input signal is Low for more than 1.5 sec while the module is turned on, the Module will be turned off.



< Picture 6.4.1 >

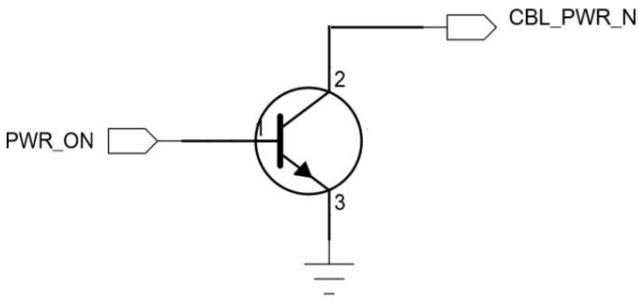
Tact type switch can be used to the module Power on/off design Power Key. Connect the switch to the CBL_PWR_N pin as shown in Picture 6.4.2.



< Picture 6.4.2 >

When CBL_PWR_N pin is high input signal for 0.5 sec or 1.5 sec, it must be designed using a N-ch TR or FET to turn on/off the power. Refer to the picture 6.4.3.

CBL_PWR_N pin has internally 0.8V~ 1.0V pull-up.



< Picture 6.4.3 >

To design a power on without using power key or GPIO control, connect a pull-down resistor to CBL_PWR_N pin. In this case, the module does not operate in PSM mode.

6.5. UART Level Shifter

UART voltage level of the Module is 1.8V. UART Level sifter must be used to connect to other UART voltage levels. It is recommended that UART Level shifter has control pin(enable/disable).

The module provides two power source.

(1) VREG_L11_1P8

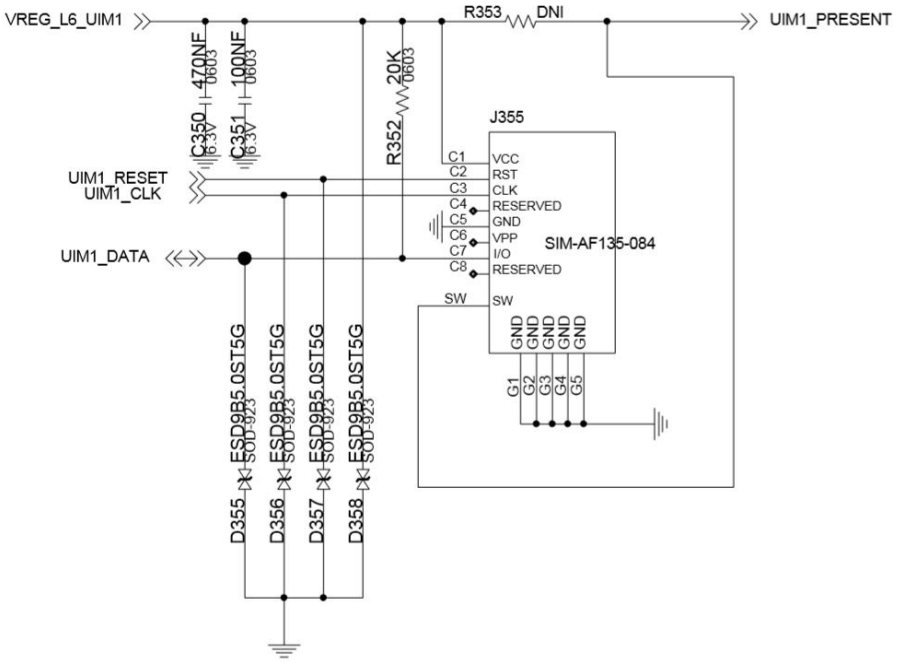
In PSM mode, VREG_L11_1P8 is turned off. In other mode, VREG_L11_1P8 is always on.

(2) VREG_L13_2P85

In PSM mode and Sleep mode, VREG_L13_2P85 is turned off.

6.6. USIM Socket

UIM1_PRESENT pin(pin M4) is used to detect the insertion and removal for a SIM device in the SIM socket. When the SIM is inserted, the UIM1_PRESENT pin will transition from a logic 1 to a logic 0 state. It is recommended to ESD protection IC as TVS diode



< Picture 6.6 >

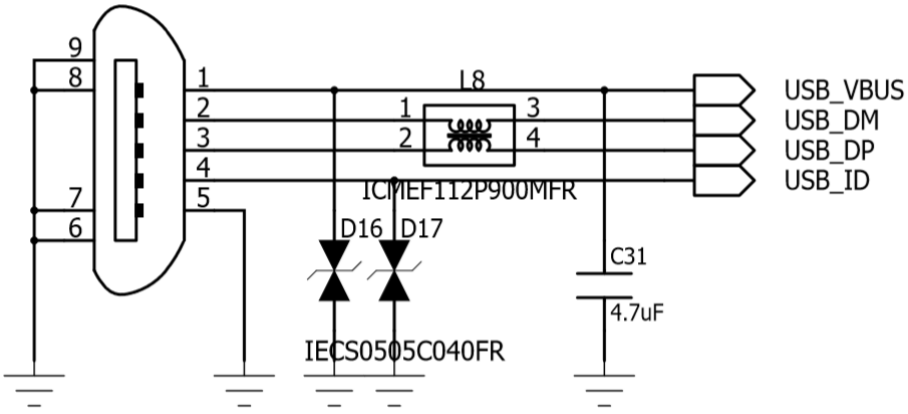
6.7. USB connection

USB_VBUS pin, USB_DP pin and USB_DM pin must be connected for a debugging purpose even if not used by the end application and USB interface.

It is recommended that the input signal of USB_VBUS is capable of on/off control in order to minimize the current consumption of the module. When USB VUSB input signal is supplied, sleep mode cannot be entered. When not in sleep mode, the current consumption is from 20mA to 30mA.

It is recommended to connect common mode ESD to USB interface lines.

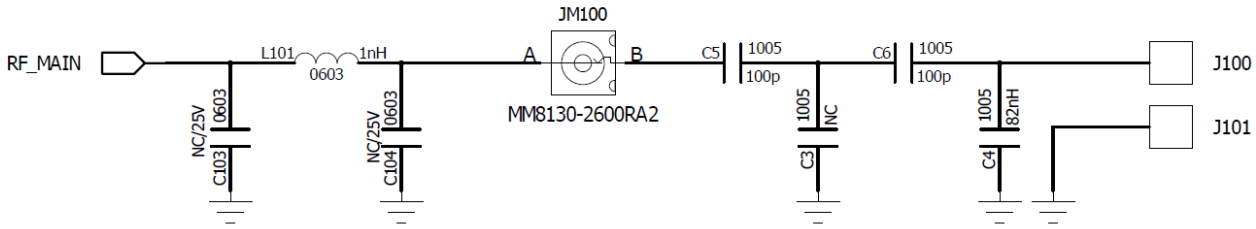
The impedance of USB differential trace is 90 Ω.



< Picture 6.7 >

6.8. Antenna Block

It is recommend to use RF connector(JM100) between ANT_MAIN pin(pin B1), ANT_MIMO pin(pin P3) or ANT_GPS pin(pin N1) and Antenna connector. Rout the trace between ANT pin and RF connector as short as possible.

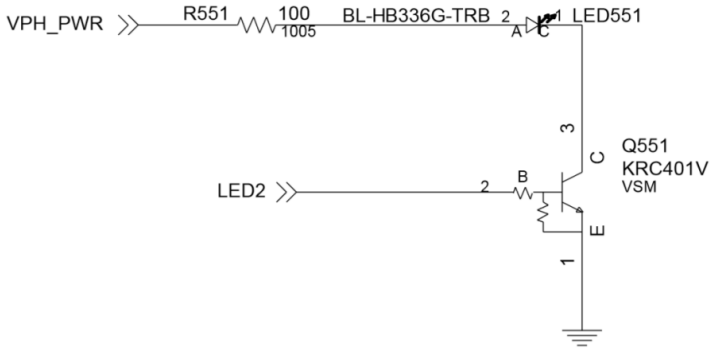


< Picture 6.8>

If the trace between ANT pin and RF connector is long, it is recommended to use RF coaxial cable.

6.9. Status LED

Three GPIOs(pin B13,pin M12,pin N12) are for LED control. LED control circuit must be designed using TR or FET for sink current.



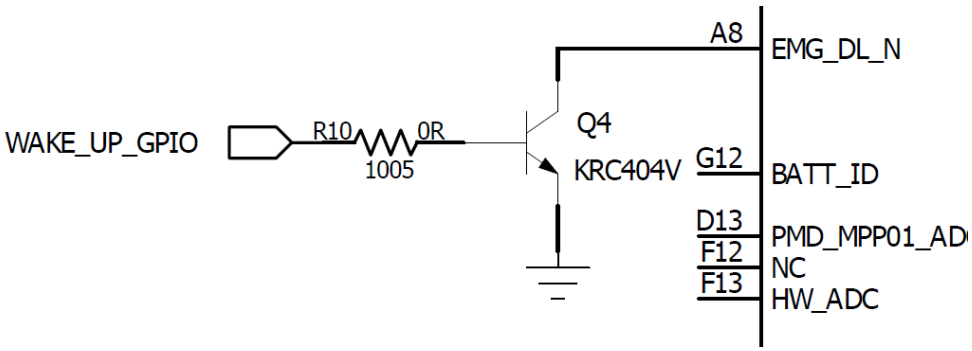
< Picture 6.9>

6.10. Wakeup interrupt GPIO

When the input signal is Low while the module is in sleep mode, the Module will be wake-up.

EMG_DL_N pin(pinA8) has internally 1.8V pull-up.

When ENG_DL_N pin is high input signal(over 1.8V), it must be designed using a N-ch TR or FET to turn on/off the power



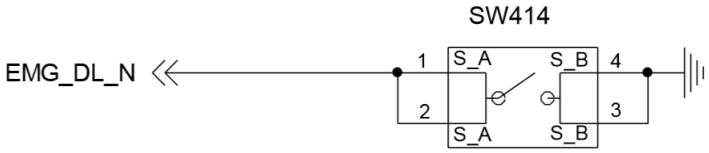
< Picture 6.10>

6.11. Emergency download

EMG_DL_N pin(pin A8)=0 forces the module to Emergency download mode.

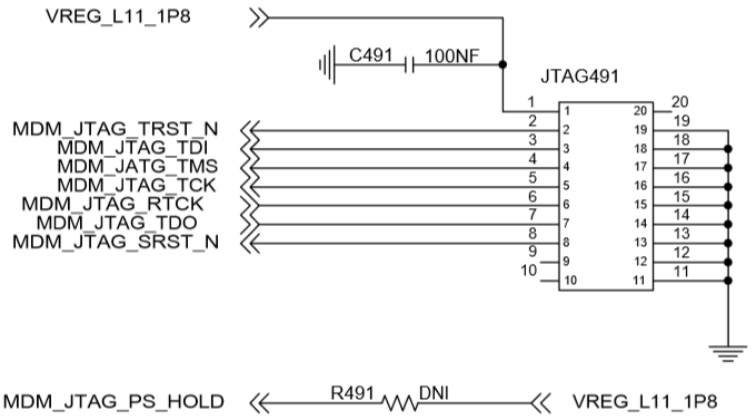
After boot, EMG_DL_N pin(pin A8) can be used for wakeup GPIO.

EMG_DL_N pin must be connected to TP or switch.



<Picture6.11>

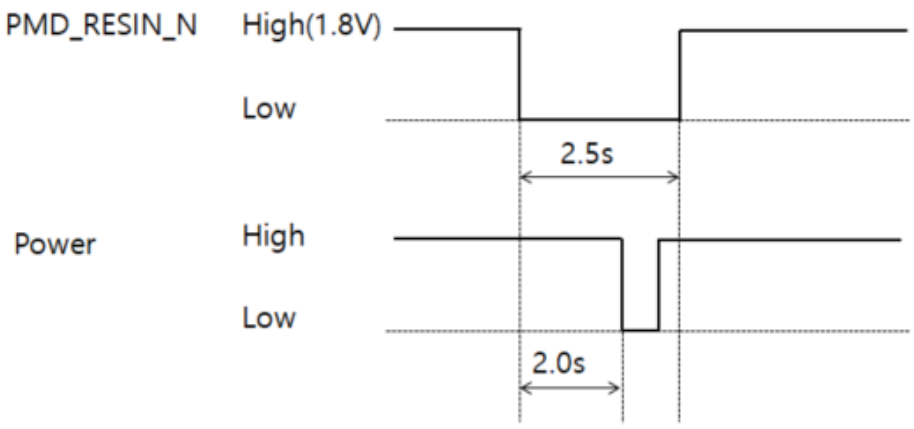
6.12. JTAG



<Picture6.12>

6.13. RESET

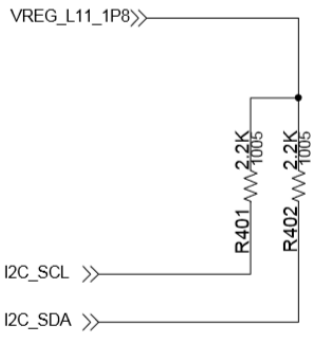
Asynchronous PMD_RESIN_N pin(pin E13), active low. Whenever this pin is active, the modem will immediately be placed in a Power On reset condition. PMD_RESIN_N pin has internally 1.8V pull-up.



<Picture6.13>

6.14. I2C Interface

The I2C interface is used for controlling peripherals inside the module. If I2C interface are used, pull-up registers are required in the customer board



<Picture6.14>